UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,154	09/08/2003	Mark L. Burgener	PER-005-PAP	5658

7590 08/10/2005

JAQUEZ & ASSOCIATES
Suite 1000
6265 Greenwich Drive
San Diego, CA 92122-5916

EXAMINER	
ENGLUND, TERRY LEE	
ART UNIT	**PAPER NUMBER**
2816	

DATE MAILED: 08/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/658,154	BURGENER ET AL.
	Examiner	Art Unit
	Terry L. Englund	2816

-- *The MAILING DATE of this communication appears on the cover sheet with the correspondence address* --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *11* is/are allowed.

6)☒ Claim(s) *1-10, 12-25, and 27-67* is/are rejected.

7)☒ Claim(s) *26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 April 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *04042005*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment/Drawings/IDS

The amendment, drawings, and IDS submitted on Apr 4, 2005 have been reviewed and considered with the following results:

The replacement sheet for Fig. 1 overcame its objection, and the applicants' comments on page 18 of the amendment overcame the objection to Fig. 2 by indicating the figure "contains material that is not known to be in the prior art. The architecture is "basic" only in that it omits switching details." Therefore, the drawing objections described in the previous Office Action have been withdrawn.

The amended abstract and paragraphs overcame their respective objections, which have now been withdrawn.

The amended claims addressed/corrected all but two of the claim objections described on pages 3-5 of the previous Office Action. The objections related to claims 12/14 and 39 have been maintained, and are described later under the appropriate section. Therefore, all of the other previous Office Action's objections to the claims (e.g. to claims 2, 10, 26-27, 32, 35, 37, 45, 47, 49-59, 62-65, and 67) have been withdrawn. However, after reviewing the claims, various concerns were noted (e.g. some related to amended changes; and others were inadvertently overlooked and/or not described in the previous Office Action). These are described later under the appropriate section.

To simplify matters with respect to which rejections of claims 3-9, 12-27, 31-32, 34-39, 41-42, 46-47, 52, 56, and 60-67 under 35 U.S.C. 112 (described on pages 5-9 of the previous Office Action) have been overcome, and which were not, all those previous Office Action

rejections have now been withdrawn. The amended claims did successfully address/correct some of those rejections (e.g. claims 3 and 4 with respect to the "circuitry"). However, not all of the rejections were addressed/corrected satisfactorily (e.g. claim 14 with respect to "circuitry" for limiting current), or even addressed (e.g. claim 19 "a second charge pump stage"). Also, some of the amended claims created their own new concerns. Therefore, this Office Action describes all known active rejections under 35 U.S.C. 112 later under the appropriate section. Some of these rejections are basically carried over from the previous Office Action, some are modified versions of the previous rejections with respect to amended changes, and some identify new rejections related to amended changes.

The prior art rejections described in the previous Office Action will now be addressed with respect to the applicants' amendment.

Amended claims 1 and 18 overcame the previous Office Action's rejections of claims 1-2, 10, and 18 under 35 U.S.C. 102(b) with respect to Tasdighi et al. These rejections have been withdrawn because Tasdighi does not show a ring oscillator (with no more than three driver sections) as now recited within claim 1, and the previous rejection did not consider the passive coupling, without conveying substantial transfer current, as now recited with claim 18. However, claims 1-2 and 10 are now rejected under 35 U.S.C. 103(a), and the 35 U.S.C. 102(b) rejection of claim 18 of claim 18 has been modified. These rejections are described later under the appropriate section.

Amended claims 1 and 18 also overcame the previous Office Action's rejections of claims 3-9, 19-22, and 22 under 35 U.S.C. 103(a) with respect to Tasdighi et al./Hara et al. Those rejections have been withdrawn because neither Tasdighi nor Hara clearly shows a ring

oscillator (with no more than three driver sections) that was being used as the charge pump clock generating circuit as now recited within claim 1, and the previous rejections did not consider the passive coupling, without conveying substantial transfer current, as now recited with claim 18. However, claims 19-22, and 22 are now rejected with respect to Tasdighi/Hara based on the modified rejection of claim 18.

However, due to the numerous amended changes, and related objections and rejections created by them, trying to account for the prior art rejections described in the previous Office Action with respect to the present set of claims is not time efficient. Therefore, all the previous Office Action's prior art rejections have been withdrawn, and this Office Action describes prior art rejections that are known to be presently active. The rejections are described later under the appropriate section.

The prior art references cited on the IDS submitted Apr 4, 2005 were reviewed and considered. Although they all relate to some type of charge pump circuit, and each shows/ discloses a capacitor, only three of these references show and/or disclose ring oscillators, and none of them show the details of all limitations (e.g. current starved drivers, or current limited sections) as recited within each independent claim. [Note: The month of reference 11 was changed to address a typo ("03" should have been --05--).]

Claim Objections

Claims 12-17, and 39 remain objected to because of the following informalities: To minimize possible confusion with respect to "an active driver" in claim 12 (line 7) with "a plurality of active driver circuits" in claim 14 (line 2), it is suggested the line 7 phrase in claim 12 be changed to --at least one active driver circuit--. Claims 13-17 carry over the objection

from claim 12. The term --the-- should be added prior to both "source" and "sink" on line 1 of claim 39 since those currents were previously recited within claim 36 (and claim 37). Appropriate corrections are required.

Claims 1-10, 12-20, 24-26, 28, 31, 39, 42, 44, 51-52, 55, and 64 are objected to because of the following informalities: Claim 1, line 14 should have --the-- added prior to "voltage" since the "voltage at the driver section output" was already described on lines 12-13 of the same claim. It is believed "a rate" on line 4 of both claims 3 and 4 should be --the rate-- since the associated phrasing relates to "a rate of rise" and "a rate of fall" already recited on lines 12 and 14, respectively of claim 1. Claim 7, line 1 should have --the-- added prior to "corresponding" to improve word flow, and to clearly relate the coupling circuits back to those already described on lines 1-2 of claim 6. Claim 12, lines 11 and 13 should have --the-- added prior to "source current" and "current sunk", respectively to more clearly refer back to the "source current and sink current" recited on lines 7-8 of the same claim. Since claim 12 already recites the source and sink currents, it is suggested claim 17, line 2 have --the-- added prior to "source and sink currents" to more clearly refer them back to the currents in claim 12. It is suggested "all" on lines 13 and 16 of claim 18 be changed to --each-- to correspond to "<u>each</u> of the source switching devices" now cited on lines 11-12 of the same claim. To relate claim 24's switching devices on line 11 back to those already identified on lines 4 and 7, it is suggested the phrase "a source switching device or to an output switching device" be changed to --at least one of the one or more source switching devices or the one or more output switching devices--. Related to this objection, it is also suggested "a source switching device control node" and "an output switching device control node" of claim 25 (lines 2-3 and 4) be modified to clearly relate to the control

nodes and switching devices already recited within claim 24 since clear relationships between elements within each claim, and within related claims, will minimize possible confusion. Also, to minimize possible confusion with respect to what claim 26's "a switching device" and "it" actually refer to, it is suggested "a switching device to which it is coupled to" on lines 2-3 of claim 26 be changed to --the corresponding switching device, to which the biasing circuitry is coupled, to--. This will help identify the device with one of the source or output switching devices recited in claim 24, and that particular device is substantially nonconductive. Otherwise, the phrase could indicate claim 26 is implying some other switching device, not already identified within the claim's chain of dependency. To minimize possible confusion, it is suggested "("TCCS") circuit is a" on line 4 of claim 28 be changed to --("TCCS") circuit refers to a type of -- to more clearly relate the circuit to "a discharging TCCS circuit' (claim 28, line 6) and "a charging TCCS circuit" (claim 29, line 2). Claim 31, line 1 "all TCCS circuit" should be --all of the TCCS circuits-- or --each of the TCCS circuits-- to refer back to the discharging/charging TCCS circuits of claims 28/29. Since claim 37 already describes "limiting the source currents and the sink currents", it is suggested --the-- be added prior to both "source" and "sink" on line 1 of claim 39. Similar to claim 28 above, it is suggested "("TCCS") circuit is a" on line 4 of claim 42 be changed to --("TCCS") circuit refers to a type of -- to more clearly relate the circuit to "a discharging TCCS circuit" (on line 6). Since claim 43 now cites section "d)", it is suggested "d)" on line 2 of claim 44 be changed to --e)-- to minimize possible confusion. Since claim 49 already cites a "voltage source" (e.g. see lines 2 and 7), it is suggested "a" on line 1 of claim 51 be changed to --the--. To minimize possible confusion with respect to a discharging switch and a "discharging switch device", it is suggested "device" be deleted from

both lines 9 and 14 of claim 52. [For example, see "TC discharging switches" on lines 4-5, and "second TC discharging switch" on lines 11 and 13 of the same claim.] To more clearly relate the various switches of claim 55 back to those within claims 49 and 54, it is suggested --of the-- be added prior to "TC" on both lines 2 and 3 of claim 55, and "switch" on the same lines be changed to --switches--.

Claim 64, line 3 "a common" should be --the common-- to clearly relate back to "a common" recited on line 2 of the same claim.

Dependent claims carry over an objection(s) from any claim(s) upon which they depend. Appropriate corrections are required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 10, 12-15, 19-21, 27-28, 34-36, 39, 41-43, 45-48, 50-53, 56, 60, 62-63, and 65-66 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which the applicants regard as the invention. The phrase "coupling substantial charge into the transfer capacitor via the charge pump clock output" in claim 10 needs clarification. For example, does the phrasing imply the coupled charge actually comes from the clock output, or is the amount of coupled charge only controlled by the clock output? It is not clear how claim 15's "an active switch" relates to the "plurality of active switches" recited on line 4 of claim 12. For example, is the switch of claim 15 one of the switches of claim 12, or can it be referring to some other active switch? It is not clear what "substantially sine-like" means in each of claims 12, 20, and 28. Therefore, clarification is

requested that clearly explains what this "sine-like" limitation actually means. For example, the original disclosure only mentions the output voltage "may oscillate substantially rail-to-rail…and may have a significantly sine-like shape" on the last lines of paragraph 050 (see page 12). However, there is no figure, or any other original description, that clearly shows or defines what may be considered "sine-like." Therefore, if a clock generating circuit provides an output that does not have fast (or sharp) rise and fall times when alternately transitioning between high and low levels, couldn't this type of output be considered "sine-like"? Also, it is well known that a ring oscillator is basically an analog circuit, and thus its output would be "sine-like." It is not understood how the "circuitry to limit the current source capacity" and "circuitry to limit the current sink capacity" in claim 14 relates to claim 12's circuitry that limits source current and current sunk. Claim 15, line 3, "an active switch" is indefinite. For example, does this refer to one of the "plurality of active switches", or to another switch that has not been clearly identified within the claim? The use of "a second charge pump stage" in the preamble of claim 19 implies a first stage that has not been clearly identified within the claim's chain of dependency. It is not clear in claim 19 how "all of the second-source switching devices" (line 7) and "all of the second-output switching devices" (line 9) relate to the switching devices recited on lines 3 and 5 if there is only one of each. For example, does the use of "all" refer to at least two, or was "all" meant to be --each--? Similar to claim 19, it is not clear in claim 21 how "all of the source switching devices" (lines 12 and 13) relates to the "one or more switching devices" recited on line 4 if there is only one of the devices, or how "all of the output switching devices" (lines 13 and 14) actually relate to the first and second output switching devices cited on lines 6-8. For example, what if there is only one source switching device? Also, can the phrasing refer to more

than just the first and second output switching devices recited within the claim? Similar to previous claims already described, it is not clear in claim 27 how "all source switching devices" (line 1) and "all output switching devices" (line 2) relate to the switching devices recited on lines 4 and 7 if there is only one of each. For example, was --each of the-- meant instead of "all"? It is not understood how the single "a TCCS circuit" of claim 34 relates to "a TC-coupling switch ("TCCS") circuit" (lines 3-4), or to "a discharging TCCS circuit" (line 6), both recited within claim 28. Similar to claim 34 above, how do the "actively controlled TCCS circuits" of claim 35 relate to "a TC-coupling switch ("TCCS") circuit" (lines 3-4), and "a discharging TCCS circuit" (line 6), recited within claim 28? It is not understood how "a particular first clock generator driver circuit" on line 4 of claim 36 relates to "a first clock generator driver circuit is a driver circuit" recited on lines 1-2 of the same claim. For example, are both phrases referring to the exact same driver circuit, or does the first clock generator circuit comprise more than just "a first clock generator driver circuit", and does the "a particular...driver circuit" phrase refer to only one of those driver circuits? Related to claim 36's driver circuit problem above, it is not understood how claim 39's "all first clock generator driver circuits" relate to the singular "a first clock generator driver circuit", "a driver circuit", or "a particular first clock generator driver circuit" recited within claim 36. It is not clear how "a passive TCCS circuit" in claim 41 relates to "a TC-coupling switch ("TCCS") circuit" (lines 3-4), or to "a discharging TCCS circuit" (line 6), recited within claim 28. Also, if a TCCS circuit is a switching circuit controlled by a charge pump clock, as identified within claim 28, how can it be considered "passive" as claim 41 recites with the "passive TCCS circuit" phrase. Clarification is requested with respect to how the "a discharging TCCS circuit" (line 6), "a discharge common TCCS" (on lines 10-11), and "a

discharge output TCCS" (line 13) within claim 42 relate to one another. For example, was "TCCS" on each of lines 11, 13, 14, and 15 of claim 42 meant to be --TCCS circuit--, or is a "TCCS" intended to be different from a "TCCS circuit"? It is not understood how claim 45's "the driver output node" relates to "each inverting driver output node" and "each of the inverting driver output nodes" that are recited within claim 43 (e.g. see lines 5 and 8, respectively). For example, is one capacitor coupled to each output node; is each output node coupled to a corresponding capacitor; or is the capacitor coupled only to one particular output node that probably provides the clock output? The coupling of the TC to the output supply "via a plurality of TC discharging switches" in claim 50 is confusing and/or misleading. This implies that more than one TC discharging switch couples the TC to the output supply. However, using the applicants' own figures as a reference, none of the figures show such a configuration. For example, even if switches 608 and 610 are considered as the discharging switches, only switch 610 actually connects TC 606 to output supply Vo-. Similar to the reasoning described above with respect to claim 50, the coupling of the TC to the voltage source "via a plurality of TC charging switches" in claim 51 is confusing and/or misleading. This implies that more than one TC discharging switch couples the TC to the voltage source. However, as shown in the applicants' own Fig. 6, only switch 602 actually couples the TC 606 to voltage source Vin+. Claims 52 (lines 4-5) and 53 (line 2) each has the same type of problem as respective claims 50 and 51, with respect to a plurality of switches coupling the TC to either the output supply or the voltage source. It is not clear in claim 56 how "<u>each actively controllable</u> TC charging switch" and "<u>each actively controllable</u> TC discharging switch" corresponds to the switches recited within claim 49. For example, is each switch inherently "actively controllable", or can these be

referring to other switches that are not clearly identified within the claim's chain of dependency, since claim 49 only cites a single "TC discharging switch" and a single "TC charging switch"? Or was --the TC-- meant instead of "each actively controllable TC"? Consistent labeling throughout the claims would minimize this confusion. The addition of "the output" in claim 60 (lines 2, 5, and 9-10) is confusing. For example, what does "the output" actually refer to, the "output supply" or the "clock output"? The "additional second TC charging switch" of claim 63 is misleading and/or confusing. For example, where in the applicants' own figures is it shown, or where is it clearly disclosed, that there can be more than one switch coupled between the TC and the source voltage? For similar reasons, the "additional second TC discharging switch" of claim 65 is misleading and/or confusing. For example, where in the applicants' own figures is it shown, or where is it clearly disclosed, that there can be more than one switch that couples the TC to the output supply? It is not clear how "each actively controllable TC coupling switch" of claim 66 relates to the charging and discharging switches of claim 60. For example, is each switch within claim 60 inherently an "actively controllable TC coupling switch", or can claim 66's "each actively controllable TC coupling switch" be referring to switches other than the single "TC charging switch" and "TC discharging switch" of claim 60? Again, consistent labeling throughout the claims would minimize confusion.

Claim 13 recites the limitation "the driver output node" in line 2 with insufficient antecedent basis for this limitation now within the claim's chain of dependency. For example, how does this "output node" now relate to the "active driver circuit" and/or "charge pump clock output" from claim 12?

Claim 43 recites the limitation "the driver circuit" in line 8. There is now insufficient antecedent basis for this limitation in the claim's chain of dependency.

Claims 46 and 47 each recites the limitation "the discharging switch" on line 3 and 2, respectively. There is insufficient antecedent basis for this limitation in either claim. Was --the discharging switch circuit-- meant, or are the switch and circuit distinctly different from one another?

Claim 48 recites the limitation "the first charge pump output" in line 1 with insufficient antecedent basis for this limitation in the claim. How does this output relate to the various output nodes identified within claim 43, and to its "first charge pump clock output"?

Claim 60 recites the limitation "the output" in line 2 with insufficient antecedent basis for this limitation in the claim. For example, is this an output of the integrated circuit, or is it related to either the output supply, or one of the first/second clock outputs?

Claim 62 recites the limitation "the switch device" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim 18 is rejected under 35 U.S.C. 102(b) as being anticipated by Tasdighi et al. (Tasdighi), a reference cited in the previous Office Action. Fig. 2 of Tasdighi shows a charge pump apparatus for generating output voltage supply Vout, wherein the apparatus comprises

transfer capacitor C1; a plurality of transfer capacitor coupling switches SW1,SW2 with each switch effectively switchable between conducting and nonconducting states under control of a charge pump clock output from charge pump clock generating circuit 24. Coupling switches SW1 and SW2 can each comprise the CMOS inverter shown in Fig. 3 (e.g. see column 3, lines 37-43), wherein transistors 26 and 27 can each be considered a distinct switching device. One of ordinary skill in the art would understand the operation of Tasdighi's circuit, which is also described on column 3, lines 16-36. Transfer capacitor C1 charges when switches SW1,SW2 couple the upper terminal of C1 to voltage source Vin and its lower terminal to Gnd, allowing transfer current to charge transfer capacitor C1 from voltage source Vin; and discharges when the switches couple the upper terminal to Gnd and its lower terminal to output voltage supply Vout, allowing current to transfer from transfer capacitor C1 to output voltage supply Vout. Therefore, one of ordinary skill in the art would know the transfer capacitor is alternately charged and discharged in accordance with the clock output. The charging would occur during period first times, and the discharging would occur during periodic second times that are not concurrent with the first times (e.g. 26 and 27 are not both fully conducting, or fully off, at the same time). [Note: The actual conduction and nonconduction periods, and the connections of the CMOS inverter in each switch SW1,SW2, will depend on if the charging operation is desired when the clock output is high, and the discharging operation is desired when the clock output is low. If the opposite operation was desired, PMOS 27 and NMOS 26 of the CMOS inverter would be reversed with respect to their connections to Vin, Gnd, and/or Vout.] Since the charge pump clock output of oscillator 24 is not shown with any intervening elements between it and the control nodes of each switch SW1,SW2 (i.e. switching devices 26 and 27), the single-phase

charge pump clock output is considered as being coupled passively to the control nodes of the switching devices. [Note: A signal line is considered one type of a passive element, that can have parasitic capacitive, or inductive, characteristics related to the line.] Since the clock output is coupled to the gates of MOS transistors 26 and 27, even if they do have some leakage current associated within them, there will be no substantial transfer current conveyed, and claim 18 is anticipated.

Claim Rejections - 35 USC § 103

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 10, 12, 14, 16, 43-44, 48-51, 53, and 57-58 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi et al., a reference cited in the previous Office Action, in view of Yamauchi, a reference found during another search. Fig. 2 of Tasdighi shows a charge pump apparatus for generating output voltage supply Vout, wherein the apparatus

comprises transfer capacitor C1; a plurality of transfer capacitor coupling switches SW1,SW2 with each switch effectively switchable between conducting and nonconducting states under control of a charge pump clock output from charge pump clock generating circuit 24. Coupling switches SW1 and SW2 can each comprise the CMOS inverter shown in Fig. 3 (e.g. see column 3, lines 37-43), wherein 26 and 27 can also be considered a distinct transfer capacitor coupling switch. One of ordinary skill in the art would understand the operation of Tasdighi's circuit, which is also described on column 3, lines 16-36. Transfer capacitor C1 charges when switches SW1,SW2 couple the upper terminal of C1 to voltage source Vin and its lower terminal to Gnd; and discharges when the switches couple the upper terminal to Gnd and its lower terminal to output voltage supply Vout. Therefore, one of ordinary skill in the art would know the transfer capacitor is alternately charged and discharged in accordance with the clock output. The charging would occur during periodic first times, and the discharging would occur during periodic second times that are not concurrent with the first times (e.g. transistors 26 and 27 within its respective switch SW1 or SW2 will not both be full on, or off, at the same time). However, the Tasdighi reference does not clearly show or disclose charge pump clock generating circuit 2 comprising a ring oscillator with no more than three inverting driver sections, or circuitry for limiting current at a driver section's output. Fig. 5 of Yamauchi shows/discloses charge pump 37 receiving charge pump clock output CLK from charge pump clock generating circuit 39, which is clearly identified as a ring oscillator. Figs. 6 and 7 both show examples of this ring oscillator, wherein each figure shows it can comprise only three inverting driver sections. Therefore, one of ordinary skill in the art would understand Yamauchi provides support for the use of controlling a charge pump with a ring oscillator with an odd number of

driver sections, which includes three sections. As such, it would have been obvious to one of ordinary skill in the art to use Yamauchi's ring oscillator 39 to provide its charge pump clock output CLK to the plurality of transfer capacitor coupling switches SW1,SW2 of Tasdighi. Using a three inverting driver section version of Yamauchi's Fig. 7, it has circuitry 49 configured as an active current limit to limit a rate of rise of voltage at each driver section's output, and circuitry 47 configured as an active current limit to limit a rate of fall of voltage at each driver section's output. Since the plurality of Tasdighi's transfer capacitor coupling switches will be under control of the particular charge pump clock output CLK (i.e. the output of the final driver section of the ring oscillator), claims 1 and 2 are rendered obvious. The use of a ring oscillator with only three driver sections will require fewer elements, take up less area, and consume less overall current, than a ring oscillator having a higher, odd number of driver sections. Deeming the line coupling the clock output from charge pump clock generating circuit (24 of Tasdighi; Fig. 7 of Yamauchi) to the control nodes of transistors 26,27 as coupling circuitry, the signal will be coupled to each coupling switch without increasing the rise of voltage rise or fall, thus rendering claims 3-4 obvious. Since transfer capacitor C1 will be periodically coupled between voltage source Vin and Gnd in response to the charge pump clock output in order to charge, a substantial charge will be coupled into transfer capacitor C1 during those periods, rendering claim 10 obvious. One of ordinary skill in the art would realize switches SW1 and SW2 of Tasdighi allow transfer capacitor C1 to be charged and discharged in an alternative, non-overlapping, manner. Since a corresponding CMOS inverter of Tasdighi's Fig. 3 can be used for each active switch SW1,SW2, the apparatus of Tasdighi can be interpreted as comprising transfer capacitor C1; active switch 26 can be disposed in series between transfer capacitor C1

and voltage source Vin; active switch 27 can be disposed in series between transfer capacitor C1 and output voltage supply Vout; and charge pump clock generating circuit (of Yamauchi's Fig. 7) comprises active driver circuit 43,45 configured to source current to (via 43), and sink current from (via 45), charge pump clock output CLK. The periodic switching of 43 and 45 will effectively provide a CLK waveform that can be considered substantially sine-like. Since clock output CLK will be coupled to the gates of MOS transistors 26,27 (the active switches), there will be no substantial charge from the clock output coupled from the source connections to the output connections of transfer capacitor C1. Circuitry 49 will limit the source current provided by active driver circuit 43,47 to clock output CLK, and circuitry 47 will limit the current sunk from clock output CLK, rendering claim 12 obvious. Since Yamauchi's charge pump clock generating circuit comprises a plurality of active drivers (each comprising transistors 43 and 45), and circuitry 49/47 for limiting current sourcing/sinking capacities of each active driver circuit with respect to their corresponding driver output node, claim 14 is also rendered obvious. With circuitry 49 and 47, one of ordinary skill in the art would understand that the charge pump clock generating circuit of Yamauchi is configured as a current-starved ring oscillator, rendering claim 16 obvious. Assuming only three driver stages within Yamauchi's first charge pump clock generator circuit as previously described above, and interpreting the Tasdighi/Yamauchi references in another manner, Tasdighi's transfer capacitor (TC) C1 is coupled to output supply Vout via a discharging switch (e.g. transistor 27 of Fig. 3, with respect to SW2 of Fig. 2); Yamauchi's corresponding source current-limiting circuit 49 limits the source current to each inverting driver output node of each driver stage s 43,45; corresponding sink current-limiting circuit 47 limits the sink current drawn from each inverting driver output node; and the inverting

driver output node of the last of the three inverting driver stages (of the first charge pump clock generator circuit) is first charge pump clock output CLK. This renders claim 43 obvious. Since TC C1 is coupled to source voltage Vin via a charging switch (e.g. transistor 26 of Fig. 3, with respect to SW1 of Fig. 2) controlled by second charge pump clock output CLK, during charge periods alternating nonconcurrently with the discharge periods, claim 44 is rendered obvious. Deeming the lines, going to the control nodes of the transistors 26 and 27 shown within Tasdighi's Fig. 3, as one type of network, first charge pump output CLK is coupled as a signal to the control node of the discharging switch circuit, and claim 48 is rendered obvious. Since single phase charge pump clock output CLK is passively coupled (e.g. coupled by a straight line with no intervening elements) to the control nodes of the charging/discharging switches (e.g. see Tasdighi's transistors 26,27 shown in Fig. 3, with respect to SW1,SW2 shown in Fig. 2), and the gate of each MOS transistor will substantially isolate transfer capacitor (TC) C1 of Tasdighi from Yamauchi's clock output CLK, claim 49 is rendered obvious. If one of transistors 26 and 27 of each of SW1 and SW2 is considered a discharge switch, and the other transistor is considered a charging switch, then there will effectively be a plurality of TC discharging switches, and a plurality of TC charging switches. For example, the charging switches would correspond to those switches coupling C1 between Vin and Gnd, allowing transfer capacitor C1 to charge, wherein the discharging switches would correspond to those switches coupling C1 between Gnd and Vout. Therefore, these plurality of discharging and charging switches render claims 50 and 51, as well as claim 53, obvious. Transistors 49 and 47 of Yamauchi make up circuitry that effectively reduces voltage change rates during both positive and negative transitions of charge pump clock output CLK since those elements reduce, or limit, the amount

of current allowed to flow to the output node. Therefore, claim 57 is rendered obvious. Since Yamauchi's charge pump clock generator circuit (shown in Fig. 7) has at least one driver circuit (e.g. each set of transistors 43,45 can be considered a driver circuit), and transistors 49 and 47 limit the currents output from each driver circuit, claim 58 is rendered obvious.

Apparatus claims 19, and method claim 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi (or Tasdighi/Yamauchi) as applied to their respective apparatus claim 18, and method claim 49 above. Although the reference(s) read on the limitations of claims 18 and 49 as previously described above, the reference(s) do not show or disclose a second charge pump stage of claim 19, or second TC, second TC charging switch, second output supply, and second TC discharging switch of claim 54. However, it would have been obvious to one of ordinary skill in the art to add a second charge pump stage/apparatus to the charge pump apparatus of claim 18, or add the elements related to the method steps of claim 49. It could have the same basic structure as Tasdighi's Fig. 2, wherein the second charge pump stage could be coupled in parallel to the charge pump apparatus, and both would receive the same charge pump clock output. Therefore, the second transfer capacitor C1 (of the stage) would be charged at the same time as C1 of the charge pump apparatus, and it would be discharged at the same time C1 of the charge pump apparatus is discharged. The first and second voltage sources would be Vin, and the first and second output voltage supplies would be Vout. Therefore, claim 19 is rendered obvious. This obvious type change would couple a second TC to a second voltage source via a second TC charging switch controlled by the charge pump output, and also couple the second TC to a second output supply via a second TC discharging switch controlled by the charge pump clock output as recited within claim 54, thus rendering that claim obvious. The coupling of two

identically structured charge pump stages in parallel, both being controlled by the same clock output, would provide one known means for providing the output voltage supply Vout with twice the current a single stage would provide. That extra current could be used if load 22 requires, or is changed to require, more current than a single stage can provide by itself. The first/second voltage sources would be equal, and the first/second output supplies would be equal.

In so far as being understood, claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi as applied to claim 18 above, and further in view of Yamauchi. Although the Tasdighi circuit and operation are understood to read on the basic limitations of claim 18 as described above, the reference does not show or disclose circuitry configured to reduce voltage change rates of positive and negative transistor so the charge pump clock output voltage is substantially sine-like. It would have been obvious to one of ordinary skill in the art to replace Tasdighi's generic type charge pump clock generating circuit 24 with a specific circuit. Yamauchi shows generic type charge pump clock generating circuit 39 in Fig 5 that provides alternating clock signal CLK to charge pump 37. Fig. 7 of Yamauchi shows details of one example of such a clock generating circuit. Therefore, it would have been obvious to use Yamauchi's Fig. 7 clock generating circuit in place of Tasdighi's circuit 24. With Yamauchi's clock generating circuit, elements 49 would be circuitry that reduces positive transitions of clock output CLK, and elements 47 would be circuitry that reduces negative transistors of clock output CLK. Since clock output CLK will be a periodic signal, and a ring oscillator is basically an analog type circuit, the output voltage of CLK can be considered substantially sine-like, rendering claim 20 obvious.

In so far as being understood, claims 28-33, 36, and 40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi in view of Tamauchi, both references cited in various claim rejections described above. Interpreting the Tasdighi/Yamaushi references in a different manner, SW2 of Tasdighi's Fig. 2 will couple transfer capacitor (TC) C1 to output supply Vout during discharge periods via a discharging TCCS circuit (e.g. transistor 27 of Fig. 3), and Yamauchi's elements 49 and 47 will actively limit the effective rate of voltage change of first charge pump clock output CLK during positive and negative transitions so that clock output CLK is substantially sine-like. This renders claim 28 obvious. SW1 will couple TC C1 to source voltage Vin via a charging TCCS circuit (e.g. transistor 26 of Fig. 3) under control of second charge pump clock output CLK during charge periods that nonoverlappingly alternate with the discharge periods (e.g. complementary periods), and Yamauchi's elements 49 and 47 will actively limit the effective rate of voltage change of second charge pump clock output CLK during positive and negative transitions, thus rendering claim 29 obvious. Since first charge pump clock output CLK is the second charge pump clock output CLK, claim 30 is also rendered obvious. Since all of Tasdighi's TCCS circuits 26,27, within each of SW1,SW2, will each be controlled by clock output CLK, claim 31 is rendered obvious. During a charging period determined by charge pump clock output CLK, TC C1 will be connected to source voltage Vin by the charging TCCS circuit (e.g. transistor 26 of Fig. 3) within SW1, thus rendering claim 32 obvious. Yamauchi's elements 49 and 47 can also be considered one type of current limiting circuit that limits the current drive capacity of charge pump clock output CLK, rendering claim 33 obvious. The last stage driver circuit providing clock output CLK of Yamauchi is a particular first clock generator driver circuit 43,45 incorporated in a first clock generator circuit (e.g. Fig. 7

of Yamauchi), wherein its first current limiting circuit 49 limits source currents from the particular first clock generator driver circuit 43,45, and second current limiting circuit 47 limits the sink currents in the particular first clock generator driver circuit 43,45. Therefore, claim 36 is rendered obvious. First current limiting circuit 49 comprises a current mirror device (e.g. see related transistors 53,55 and 49), and second current limiting circuit 47 effectively comprises a different current mirror (e.g. all three transistors 47 each receive the same control voltage Vcon). It would be obvious to one of ordinary skill in the art that Yamauchi's charge pump clock CLK is generated by a current-starved ring oscillator (e.g. see Fig. 7), wherein it can have only three inverting driver sections coupled in a ring, rendering claim 40 obvious. A ring oscillator with only three driver sections would comprise fewer elements, and consume less current, than a ring oscillator comprising an number (greater than three) of driver sections.

Claims 1-9, 12, 16, 18, 20, 22, 24-41, 43-51, 53-61, and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi et al. (Tasdighi) in view of Hara et al. (Hara). As previously described above with respect to the Tasdighi/Yamauchi rejections, Fig. 2 of Tasdighi shows/discloses a charge pump apparatus for generating output voltage supply Vout, wherein the periodic first/second times are understood. However, the reference does not clearly show or disclose a ring oscillator with only three driver sections; the rise/fall rate current limiting circuitry; the current source/sink limit devices, circuitry configured to limit (source and/or sink) currents conducted by an amplifying driver circuit, or capacitive coupling circuit(s) to a coupling switch. However, Tasdighi does disclose the clock output of oscillator 24 can be changed by various ways (e.g. see column 4, lines 47-55), and the oscillator "could be a ring oscillator or any other known from of oscillator" (i.e. see column 5, lines 21-22). Fig. 13 of Hara shows the clock

output of ring oscillator 89d being applied to the input of a charge pump type circuit 89e. Each of Figs. 1, 4-6, 8, and 10 of Hara show different embodiments of ring oscillators that can be used as ring oscillator 89d (i.e. see column 8, lines 59-61). These embodiments are disclosed with respect to current limiting (e.g. see column 3, lines 29-50), reducing power consumption (e.g. see column 3, lines 60-62), and changing the oscillation cycle (e.g. see column 2, lines 16-19 and 36-39). Therefore, it would have been obvious to one of ordinary skill in the art to use one of Hara's ring oscillators (e.g. Fig. 6) as the oscillator in Tasdighi's Fig. 2 apparatus. [Hara's Fig. 6 ring oscillator closely corresponds to the applicants' own Fig. 4 circuit, wherein the inverters 1a-5a,1d-5d of Hara are coupled to current mirror associated transistors 1b-6b to provide limited source currents, and other current mirror associated transistors 1c-6c to provide limited sink currents.] Using a modified ring oscillator with only three driver sections, with the final stage providing particular charge pump clock output OUT to the plurality of Tasdighi's transfer capacitor coupling switches, renders claim 1 obvious since circuitry b limits the rise rate of clock output OUT, and circuitry c limits the fall rate of clock output OUT. A ring oscillator with three driver sections will still provide a charge pump clock output, and will use few elements, require less area, and consume less current, than a ring oscillator with a higher, odd number of driver sections. Since the plurality of Tasdighi's transfer capacitor coupling switches (SW1/SW2; 26,27/26,27) will be controlled by particular charge pump clock output OUT, claim 2 is also rendered obvious. If the signal path coupled between clock output OUT and the plurality of transfer capacitor coupling switches is deemed circuitry, the coupling circuitry couples the signal to each switch without increasing the rate of voltage rise or fall, rendering claims 3 and 4 obvious. The rate of rise and fall is determined by the driver sections within the

ring oscillator. The series connection of current mirror input transistors 6b and 6c allows substantially identical magnitudes of the limited source currents (via b) and sink currents (via c), rendering claim 9 obvious. Although neither reference clearly shows capacitive coupling circuit(s) to at least one transfer capacitor coupling switch, Fig. 20 of Hara shows capacitive coupling circuits (not labeled) connected to transistors 12p and 12n, which one of ordinary skill in the art would understand are types of coupling switches. Therefore, it would have been obvious to one of ordinary skill in the art to provide a respective capacitive coupling circuit between Hara's clock output OUT and the control node of each corresponding transfer capacitor coupling switch (e.g. SW1,SW2 or 26,27) of Tasdighi, thus rendering claims 5-6 obvious. The capacitive coupling circuits would provide one means for DC blocking to minimize possible transitioning errors. Since the capacitive coupling circuits provide clock output OUT to the control nodes (i.e. gates) of the coupling switches (i.e. MOS transistors), one of ordinary skill in the art would know that the capacitive coupling circuit do not conduct any substantial charge to transfer capacitor C1, rendering claims 7 and 8 obvious. The charge to transfer capacitor C1 is actually related to the drain/source connections of the coupling switches. Interpreting Hara's Fig. 6 charge pump clock generating circuit in a different manner, the generating circuit includes an active driver circuit a,d configured to source current (via a) to driver output node OUT, and sink current (via d) from the output node, wherein the generator circuit also includes circuitry b for limiting the source current, and circuitry c for limiting the current sunk. Since it is the conducting/nonconducting states of the active switches that couple charge to transfer capacitor C1, clock output OUT does not conduct any substantial charge from the source connection to the output connections. Also, since clock output OUT can be considered substantially sine-like (e.g.

alternating between high and low type levels), this interpretation renders obvious claim 12. Similar to claims 7-8, 5-6, and 9 described above, claims 14, 15, and 17 are respectfully rendered obvious. Also, claim 16 is rendered obvious because Hara's oscillator circuit is one known type of a current-starved ring oscillator. Circuitry 60,1b-5b,1c-5c of Hara's charge pump clock generating circuit limits currents conducted by each amplifying driver circuit (e.g. 1a/1d – 5a/5d), which one of ordinary skill in the art would understands will reduce the voltage change rates of clock output OUT during both positive and negative transitions. With clock output OUT passively coupled to the control nodes (i.e. gates) of the switching devices (i.e. MOS transistors), it is understood there will be substantially no transfer current conveyed by the clock output (e.g. only some possible leakage current will flow between the control node and the switching devices output). Therefore, claims 18, 20 and 22 also rendered obvious. For the same reasoning as applied before with respect to the transfer capacitor, source switching device(s), output switching device(s), and the capacitive coupling circuit(s), claims 24-27 are rendered obvious. Interpreting the Tasdighi/Hara circuitry as a method, a discharging TCS circuit (within switch SW2) of Tasdighi couples transfer capacitor (TC) to output supply Vout during discharge periods under control of first charge pump clock output OUT of Hara's ring oscillator (shown in Fig. 6); wherein 60,1b-5b1c-5c actively limit a rate of voltage change of clock output OUT during both positive and negative transitions. The alternating clock output OUT can be considered to be substantially sine-like, and claim 28 is rendered obvious. A charging TCCS circuit (with switch SW1) of Tasdighi couples transfer capacitor (TC) to source voltage Vin during charge periods under control of second charge pump clock output OUT of Hara's ring oscillator (shown in Fig. 6) that alternate nonoverlappingly with the discharge periods (e.g. provide complementary

charging and discharging); wherein 60,1b-5b1c-5c actively limit a rate of voltage change of second clock output OUT during both positive and negative transitions, rendering claim 29 obvious. First charge pump clock output OUT is the second charge pump clock output OUT, and claim 30 is rendered obvious. Since the first charge pump clock output OUT controls all the TCCS circuits (SW1,SW2 or 26,27) of Tasdighi, claim 31 is rendered obvious. By controlling when the switches become conductive or not conductive, the charge pump clock output effectively couples TC C1 to voltage source/source voltage Vin, rendering claim 32 obvious. Current limiting circuit 5b,5c limits the current drive capacity of charge pump clock output OUT, and claim 33 is rendered obvious. As previously described, first charge pump clock output OUT can be coupled to each TCS circuit by a corresponding capacitive coupling circuit, rendering obvious claims 34-35. First current limiting circuit 5b limits source currents from driver circuit 5a/5d, and second current limiting circuit 5c limits sink currents in driver circuit 5a,5d, and claim 36 is rendered obvious. Due to the current limiting relationships with respect to series connected 6b,6c, the source and sink currents have substantially identical magnitudes, and claim 37 is rendered obvious. First current limiting circuit 5b comprises a current mirror device 5b (e.g. with respect to 6b) and second current limiting circuit 5c comprises a different current mirror device 5c (e.g. with respect to 6c), rendering claim 38 obvious. 1b-5b and 1c-5c limit source and sink currents respectively to/from their corresponding driver circuits, and claim 39 is rendered obvious. Fig. 6 of Hara is one known type of current-starved ring oscillator, rendering claim 40 obvious. It would have been obvious to one of ordinary skill in the art to use a diode, or diode-connected transistor as a passive TCCS circuit to couple TC 31 to source voltage Vin or output supply Vout, rendering obvious claim 41. One of ordinary skill in the art understands a passive

device (e.g. a diode) can be used in place of an active device (e.g. a transistor), when they are to be used as a switching device that is either conductive or nonconductive with respect to a clock output signal. Since claims 43-51, 53-61, and 66-67 are obvious variations of the limitations cited in the numerous claims already rejected within the previous descriptions, it is not considered necessary to keep repeating redundant type explanations. Therefore, claims 43-51, 53-61, and 66-67 are rendered obvious for the same reasoning as previously presented with respect to the other rejected claims.

Claims 1-10, 12-20, 22-25, 27-41, 43-51, 53-61, and 66-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tasdighi et al. (Tasdighi) in view of Ito et al. (Ito). As previously described above, Figs. 2/5 of Tasdighi shows/discloses a charge pump apparatus for generating an output voltage supply Vout, wherein the rise/fall rates are limited, and the periodic first/second times are understood. However, Tasdighi does not show or disclose charge pump clock generating circuit 24 including a ring oscillator, comprising no more than three inverting driver sections; current source/sink limit devices; circuitry configured to limit (source and/or sink) currents conducted by an amplifying driver circuit/active driver circuits; capacitive coupling circuit(s) to a coupling switch; or a discrete capacitive element coupled to the driver output node. However, Tasdighi does disclose the clock output of the oscillator can be changed by various ways (e.g. see column 4, lines 47-55), and the oscillator "could be a ring oscillator or any other known from of oscillator" (i.e. see column 5, lines 21-22). Fig. 12 of Ito shows ring oscillator 70 providing clock output CLKO that can be controlled (via Vf, Vc, and the values of delay capacitors 51c-53c; see column 2, lines 5-47). Therefore, it would have been obvious to one of ordinary skill in the art to use Ito's ring oscillator 70 as the oscillator in Tasdighi's Fig. 2

apparatus. [Ito's Fig. 12 ring oscillator closely corresponds to the circuits shown in the applicants' own Figs. 4-5, wherein the inverters 51a/51b,52a/52b,53a/53b of Ito are coupled to current mirror associated transistors 58-61 to provide limited source currents, and other current mirror associated transistors 62-64 to provide limited sink currents.] Since the ring oscillator comprises no more than three inverting driver sections, current source limit device 61 limits the rise rate of clock output CLKO, and current sink limit device 64 limits the fall rate of clock output CLKO, claims 1-4 are rendered obvious. With 58-61 and 62-64 limiting the currents conducted by their respective amplifying driver circuit (e.g. 61,64 limit the currents of amplifying driver circuit 53a,53b), claims 7-8 are rendered obvious. The series connection of current mirror input transistors 58 and 57 allows substantially identical magnitudes of the limited source currents (via 59-61) and sink currents (via 62-64), rendering claim 9 obvious. It would have been obvious to one of ordinary skill in the art to provide a respective capacitive coupling circuit between Ito's clock output CLKO and the control node of each corresponding transfer capacitor coupling switch (e.g. SW1,SW2 or 26,27) of Tasdighi, thus rendering claims 5-6 obvious. The capacitive coupling circuits would provide one means for DC blocking to minimize possible transitioning errors. Since the charge of transfer capacitor C1 is controlled by the charge pump clock output, the charge into the transfer capacitor can be considered via the charge pump clock output, rendering claim 10 obvious. Interpreting Ito's Fig. 12 charge pump clock generating circuit in a different manner, the generating circuit includes an active driver circuit 53a/53b configured to source current (via 61) to driver output node CLKO and sink current (via 53b) from the output node, wherein the generator circuit also includes circuitry 61 for limiting the source current, and circuitry 64 for limiting the current sunk. This interpretation

renders obvious claim 12. Discrete capacitive element 53c is coupled to driver output node CLKO, and its connection is understood to reduce voltage rates of change at the driver output node due to the known charging/discharging characteristics of a capacitor, rendering claim 13 obvious. 51a/51b, 52a/52b, and 53a/53b are each an active driver circuit configured to source and sink currents to their corresponding driver output node; circuitry 59-61 limits the current source capacity of each driver circuit; and circuitry 62-64 limits the current sink capacity of each driver circuit, and claim 14 is rendered obvious. As previously described above with respect to claims 5-6, capacitive coupling networks can be used to coupled clock output CLKO to the control node of active switches within the charge pump apparatus, thus claim 15 is rendered obvious. Due to the current limiting transistors 59-64, the ring oscillator of Ito is configured as one known type of a current-starved ring oscillator, rendering obvious claim 16. The configuration of source current circuitry 58-61 and sink current circuitry 56, 62-64 will limit source and sink currents to substantially identical magnitudes, and claim 17 is rendered obvious. For the same reasoning as applied before with respect to prior art rejections described related to the Tasdighi/Hara references, and to prior art rejections described above with respect to claims 1-9, and 12-17 and the Tasdighi/Ito references, claims 18-20, 22-25, 27-41, 43-51, 53-61, and 66-67 are also rendered obvious. These claims are obvious variations of the numerous claims already rejected within the previous descriptions, and it is not considered necessary to keep repeating redundant type explanations.

Allowable Subject Matter

Claim 11 is allowed. There is presently no motivation to modify or combine any prior art reference(s) to ensure the second control node AC impedance is at least twice the first control node AC impedance as recited within independent claim 11.

Claims 21, 42, and 52 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action. There is presently no motivation to modify or combine any prior art reference(s) to ensure: 1) the second device area is greater than double the first device area as recited within claim 21; 2) the control node AC impedance of the discharge output TCCS is at least double the control node AC impedance of the discharge common TCCS as recited within claim 42; 3) the control node AC impedances have the relationship (i.e. second discharging switch AC impedance ≥2 * first discharging switch AC impedance) as recited within claim 52.

Claim 26 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure: 1) the capacitive coupling circuit(s) also include biasing circuitry as recited within claim 26.

Also, claims 62-65 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims. There is presently no strong motivation to modify or combine any prior art reference(s) to ensure the biasing of each capacitive coupling network as recited within claim 62 (upon which claims 63-65 depend).

Prior Art

The other prior art reference cited on the accompanying PTO-892 is deemed relevant to at least claims comprising a ring oscillator having three inverting driver sections. Although not used in any formal rejections described above, Fig. 7 of Notani shows/discloses an example of a ring oscillator having only three inverting driver sections (e.g. see column 1, lines 17-24), wherein each section has is own circuitry 63,64 that will limit the rise and fall rates of the voltage at that section's output. Therefore, this reference should also be carefully reviewed and considered since one of ordinary skill in the art would know that this ring oscillator could also be used as a clock generating circuit is numerous applications requiring a circuit for generating a clock signal.

As previously described under the Response to Amendment/Drawings/IDS section, the prior art references cited on the IDS submitted Apr 4, 2005 have been reviewed and considered.

Response to Arguments

The applicant's arguments filed Apr 4, 2005 have been fully considered but they are not persuasive. The applicant's argue that: 1) Tasdighi does not suggest a novel combination of oscillators with charge pump circuits; 2) Hara et al.'s, and Ito's, ring oscillators are for a PLL or VCO, and Hara's ring oscillator should have five or more stages; 3) all oscillators incorporated into charge pumps produce substantially rectangular output waveforms; 4) three-stage ring oscillators are known, but have not been used to drive charge pumps; and 5) the references of Tasdisghi, Hara et al., and Ito do not show or disclose the claimed limitations, and therefore the claims are nonobvious.

1-2) In response to the applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). Tasdighi discloses that a ring oscillator can be used to provide the clock signal to charge pump comprising SW1,SW2,C1. Each of the references of Hara et al. and Yamauchi shows/discloses the use of current-starved type ring oscillators for providing the clocking signals to a corresponding charge pump. For example, see the ring oscillators in Yamauchi's Figs. 6-7, which can be used to provide CLK to pump circuit 37 shown in Fig. 5. Fig. 13 of Hara et al. shows ring oscillator 89b (89d) for providing a signal to charge pump circuit 89c (89e). Hara et al.'s Figs. 1, 4, 5, 6, 8, 10, 19, and 20 each shows an example of a current-starved ring oscillator (although the disclosure does not use that label). Therefore, one of ordinary skill in the art would have no trouble understanding that a charge pump type circuit (e.g. voltage booster) can be controlled by such a ring oscillator, and their use with a charge pump is not considered novel. Although Hara et al.'s disclosure might indicate the ring oscillators are for PLL circuits, that reference also clearly shows charge pump circuits 89c and 89e receiving their control signal from ring oscillators (e.g. see Fig. 13), wherein this reference also shows specific examples of ring oscillators. Therefore, one of ordinary skill in the art would know those ring oscillators can be used with charge pump circuits (which provide a boosted output signal, such as VBB). Even if Hara disclose the ring oscillator <u>should</u> have five or more stages, there does not appear to be any reason why they cannot have only three stages. Knowing that ring oscillators (e.g. current-starved ring oscillators) can have three stages, and can be used to control charge pump circuits, one of ordinary skill in the art

would find most of the claimed limitations within the present application obvious. Also, whether a ring oscillator is shown/disclosed as being used in a PLL or a VCO, there is nothing preventing one of ordinary skill in the art from using a ring oscillator as one known means for providing a control signal to some other circuitry, such as a charge pump circuit.

3-4) The applicant's arguments fail to comply with 37 CFR 1.111(b) because they amount to a general allegation that the claims define a patentable invention without specifically pointing out how the language of the claims patentably distinguishes them from the references. Although the applicant cites all oscillators incorporated into charge pumps produce substantially rectangular output waveforms, the applicant's own disclosure and figures do not clearly support any thing different. For example, the original disclosure only mentions the output voltage "may oscillate substantially rail-to-rail…and may have a significantly sine-like shape" on the last lines of paragraph 050 (see page 12). Therefore, how does this vague description set the claimed charge pump generating circuit, with a ring oscillator, apart from other known ring oscillators? Also, the reference of Goldman shows/discloses a typical ring oscillator, having three inverters (operating in a current starved mode) connected in a ring, and that ring oscillator can be in an analog operation mode (e.g. see column 1, lines 14-27). Therefore, this reference provides sufficient background support for current-starved ring oscillators providing sine-like signals. With respect to the use of three-stage ring oscillators for driving charge pumps, a charge pump requires a control signal (or clock) to allow their switching to occur. Therefore, what actually prevents a ring oscillator, having only three stages, from providing that control? A three-stage ring oscillator will still provide an alternating signal, it will use fewer components, take up less area, and consume less current than a ring oscillator having more than three-stages.

For the reasons described above, the prior art rejections cited in this Office Action, and those in the previous Office Action, are deemed proper with respect to the broadest reasonable interpretation of the claimed limitations and prior art knowledge.

THIS ACTION IS MADE FINAL. The applicants are reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication, or previous communications, from the examiner should be directed to Terry L. Englund whose telephone number is (571) 272-1743. The examiner can normally be reached Monday-Friday from 7 AM to 3 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tim Callahan, can be reached on (571) 272-1740.

The new central official fax number is (571) 273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TLE
Terry L. Englund

24 July 2005

My Trang Ton
MY-TRANG NU TON
PRIMARY EXAMINER
8/8/05

Approved 6.26.05 TLE

Amendments to the Drawings:

Figure 1 has been amended in response to the Examiner's objections thereto by addition of the term "Prior Art" as requested. A replacement first drawing sheet incorporating these changes, together with an annotated first drawing sheet showing changes in red, are attached to this response as an appendix.

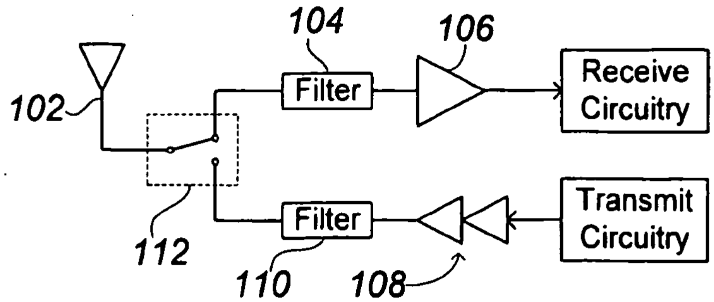
Attachments: Replacement Drawing Sheet

Annotated Sheet showing changes

-ANNOTATED SHEET SHOWING CHANGES-

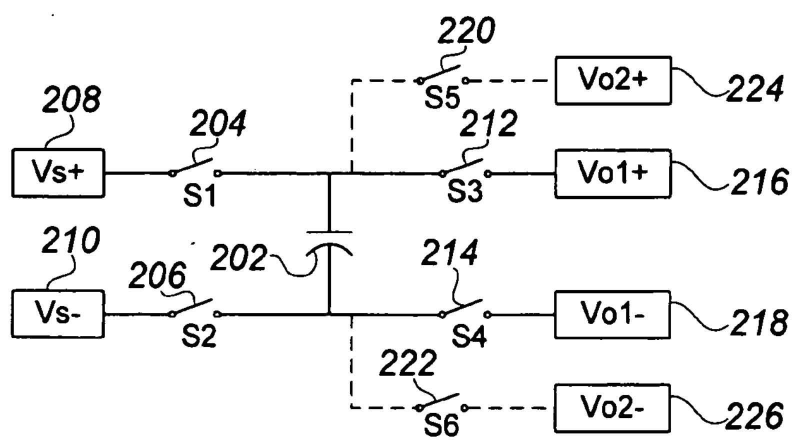
Approved
6.26.05
T.L.E

FIG. 1



(PRIOR ART)

FIG. 2



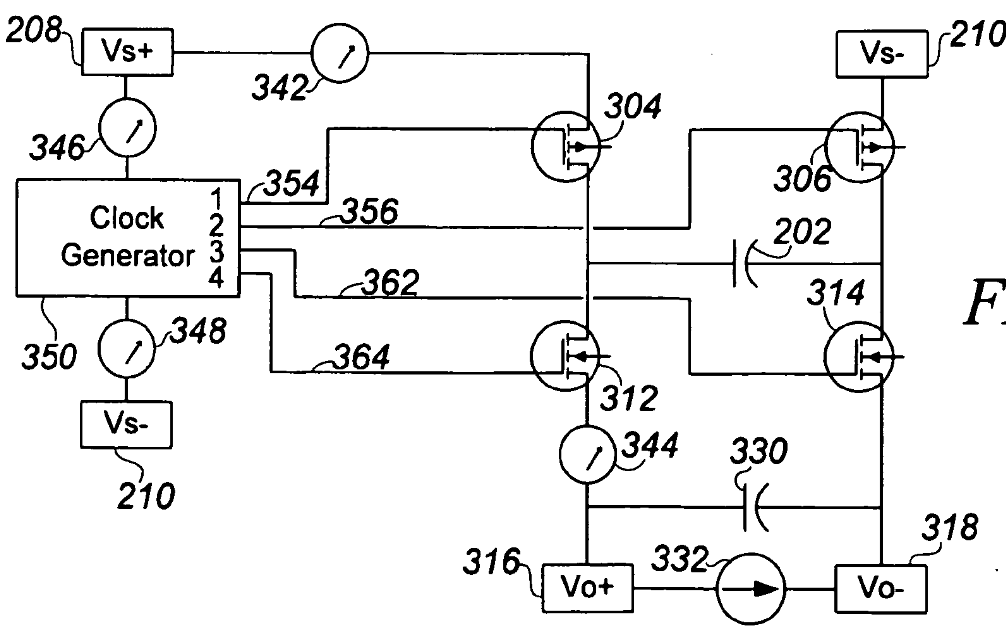


FIG. 3